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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/016,143	12/17/2001	Tetsuro Asano	492322002400	4142

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EXAMINER	
TRAN, TAN N	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 11/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/016,143	ASANO ET AL.	
	Examiner	Art Unit	
	TAN N TRAN	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 October 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 25-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7,8,10-12,25-28* is/are rejected.

7)☒ Claim(s) *6 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 25 stand rejected under 35 U.S.C. 102(b) as being anticipated by Yamashita et al. (6,124,736).

With regard to claim 25, figure 3b of Yamashita et al. discloses a first switch comprising two field-effect transistors (T200, T201) each having a source electrode, gate electrode, a drain electrode; and input terminal pad, and a common output terminal pad (O') for the two transistors (T200, T201) of the first switch, the source electrode or the drain electrode of each of the two transistors (T200, T201) of the first switch being electrically in contact with the common output terminal pad (O'); and the source electrode or the drain electrode of each of the two transistors (T200, T201) of the first switch which are not electrically in contact with the common output terminal pad (O') of the first switch being connected to the input terminal pads (IO, I1); a second switch comprising two field-effect transistors (T202, T203) each having a source electrode, gate electrode, a drain electrode; and input terminal pad, and a common output terminal pad (O) for the two transistors (T202, T203) of the second switch, the source electrode or the drain electrode

of each of the two transistors (T202, T203) of the second switch being electrically in contact with to the common output terminal pad (O); and the source electrode or the drain electrode of each of the two transistors (T202, T203) of the second switch which are not electrically in contact with the common output terminal pad (O) of the second switch being connected to the input terminal pads (IO', I1'); two control terminal pads (S,S'); two control terminal pads (S,S'), one of the two control terminal pads S' being connected to a gate electrode of one of two transistors of the first switch and a gate electrode of one of the two transistors of the second switch, and another of the two control terminal pads S being connected to a gate electrode of another of the two transistors of the first switch and a gate electrode of another of the two transistors of the second switch. (Note C200, Fig. 3b of Yamashita et al.).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5,7,8,10,11,12,26 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita et al. (6,124,736) in view of Applicant's prior art (APA) fig.1 as reasons set forth in the office action paper no.9.

With regard to claim 1, Yamashita et al. discloses a first, a second, a third and a fourth field-effect transistors (T200, T201, T202, T203), each of said transistors (T200, T201, T202,

T203) having a source electrode, gate electrode, and a drain electrode; a first, a second, a third and a fourth input terminal pad (IO, I1, IO', I1') corresponding to the first, second, third, and fourth transistors (T200, T201, T202, T203), respectively, the source electrode or the drain electrode of each of the four transistors (T200, T201, T202, T203) being connected to the corresponding input terminal pad thereof; a first common output terminal pad (O') being electrically in contact with the source electrode or the drain electrode of the first transistor (T200) and electrically in contact with the source electrode or the drain electrode of the second transistor (T201), the two electrodes of the first and second transistors which are electrically in contact with the first common output terminal pad (O') being connected to any of the input terminal pads (IO, I1, IO', I1'); a second common output terminal pad (O) being electrically in contact with the source electrode or the drain electrode of the third transistor (T202) and electrically in contact with the source electrode or the drain electrode of the fourth transistor (T203), the two electrodes of the first and second transistors which are electrically in contact with the second common output terminal pad (O) being connected to any of the input terminal pads (IO, I1, IO', I1'); a first control terminal pad (S') connected to the gate electrodes of the first and third transistors (T200, T202); and a second control terminal pad (S) connected to the gate electrodes of the second and fourth transistors (T201, T202). (Note C200, Fig. 3b of Yamashita et al.).

Yamashita et al. does not disclose a semiconductor switching circuit device formed on a substrate, each of transistors having a source electrode, a gate electrode and a drain electrode which are formed on a channel layer of the substrate.

However, APA discloses a semiconductor switching circuit device comprising a transistor formed on a substrate 1 wherein a source electrode 4, a gate electrode 3 and a drain electrode 5 of the transistor are formed on a channel layer 2. (Note fig. 1A of APA).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Yamashita et al.'s device having a semiconductor switching circuit device formed on a substrate and each of transistors of the switching circuit having a source electrode, a gate electrode and a drain electrode which are formed on a channel layer such as taught by APA because such structure is conventional in the art for forming the field effect transistor device.

With regard to claim 4, Yamashita et al. discloses a first connection connecting the first control terminal pad (S') and the gate electrode of the third transistor (T202), wherein the four transistors (T200, T201, T202, T203) are aligned in a direction forming a row of the first, second, third and fourth transistors (T200, T201, T202, T203) in this order, and wherein the connection is disposed along the row of the transistors (T200, T201, T202, T203). (Note C200, Fig. 3b of Yamashita et al.).

With regard to claims 2, 11, APA discloses the gate electrode 3 forms a Schottky contact with the channel layer 2 and the source electrode 4 and the drain electrode 5 form an ohmic contact with the channel layer 2. (Note 21-24,page 1, fig 1A of APA).

With regard to claims 3, 12, APA discloses the substrate 1 is made of a compound semiconductor GaAs and each of the transistors (FET1, FET2) is a metal-semiconductor field effect transistor. (Note fig. 1A,1B of APA).

With regard to claim 5, fig. 3(b) of Yamashita et al. disclose all the claimed subject matter except for a resistor is formed between the first control terminal pad and the gate

electrode of the third transistor. However, it would have been obvious to one of ordinary skill in the art to form a resistor is formed between the first control terminal pad and the gate electrode of the third transistor because such structure is conventional in the art for preventing the leakage of the high frequency signals through the gate. Note fig. 1B of APA is cited to support for the well know position.

With regard to claim 7, Yamashita et al. discloses a second connection connecting the second control terminal pad (S) and the gate electrode of the second transistor T201, wherein the two connections intersect each other. (Note C200, Fig. 3b of Yamashita et al.).

With regard to claim 8, Yamashita et al. discloses the first, second, third and fourth input terminal pads (IO, I1, IO', I1') are disposed on one side of the device so that each of the pads is placed next to the corresponding transistor and wherein the first and second common output terminal pads (O,O') and the first and second control terminal pads (S,S') are disposed on a side of the device opposite the side of the device of the four input terminal pads (IO, I1, IO', I1'). (Note C200, Fig. 3b of Yamashita et al.). APA and Yamashita et al. disclose all claimed invention, except the two control terminal pads are placed at both ends of the opposite side of the device and the two common output terminal pads are placed between the two control terminal pads. However, although APA and Yamashita et al. does not teach exact the place of the two control terminal pads the two common output terminal pads as that claimed by Applicant, the place differences are considered obvious design choices and are not patentable unless unobvious or expected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note in re Leshin, 125 USPQ 416.

With regard to claim 10, Yamashita et al. discloses portions of the first and second transistors (T200, T201) are disposed between the first and second input terminal pads (IO, I1,), and wherein portions of the third and fourth transistors (T202, T203) are disposed between the third and fourth input terminal pads (IO', I1'). (Note C200, Fig. 3b of Yamashita et al.)

With regard to claim 26, Yamashita et al. does not disclose each of the first and second switch comprises a single pole double throw switch.

However, APA discloses the switch comprises a single pole double throw switch. (Note line 29, page 1, fig. 1B of APA).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Yamashita et al.'s device having the switch comprises a single pole double throw switch such as taught by APA because such structure is conventional in the art for forming a high frequencies switching device that can be used in a mobile communication device.

Claims 27,28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita et al. (6,124,736).

With regard to claim 27, Yamashita et al. disclose four input terminal pads (IO,IO', I1, I1'); two common output terminal pads (O,O'); no more than two control terminal pads (S,S'). (Note C200, Fig. 3b of Yamashita et al.).

Yamashita et al. disclose all the claimed subject matter except for two single pole double throw switches, each of the switches receiving two high frequency signals through two of the four input terminals and outputting one of the two high frequency signals to one of the two common output terminals in response to a control signal received from one of the control

terminal. However, it would have been obvious to one of ordinary skill in the art to form two single pole double throw switches, each of the switches receiving two high frequency signals through two of the four input terminals and outputting one of the two high frequency signals to one of the two common output terminals in response to a control signal received from one of the control terminal because such structure is conventional in the art for forming the two-switching-element switch.

With regard to claim 28, Yamashita et al. disclose all the claimed subject matter except for the four input terminal pads receive two pairs of balanced signals, and the two common output terminal pads output one of the two pairs of the balanced signals selected by signals applied to the two control terminal pads. However, it would have been obvious to one of ordinary skill in the art to form the four input terminal pads receive two pairs of balanced signals, and the two common output terminal pads output one of the two pairs of the balanced signals selected by signals applied to the two control terminal pads because such structure is conventional in the art for forming the two-switching-element switch.

Allowable Subject Matter

3. Claims 6,9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 6,9 are allowable over the prior art of record, because none of these references disclose or can be combined to yield the claimed invention such as the resistor comprises a high

dopant concentration region as recited in claim 6, the first and second connections are disposed between the row of the four transistors and a row of the control terminal pads and the common output terminal pads as recited in claim 9.

Response to Arguments

4. Applicant's arguments filed 10/01/03 have been fully considered but they are not persuasive.

It is argued, at pages 8-10,12 of the remark, that "Yamashita's leads are not electrically in contact with the corresponding source or drain of the logic circuit device. The signals inputted through Yamashita's leads IO, IO', I1, I1', which the examiner cites as corresponding to the input terminal pads of claims 25, are not outputted from the output leads O, O' of Yamashita"; "Yamashita does not teach or suggest the feature of claim 25 that the source or drain of the transistor is electrically in contact with the common output terminal"; "the logic circuit C200 shown in Fig. 3B of Yamashita relied upon by the examiner doe not have any terminal pad for external connection"; "Applicants request the examiner to provide evidence that the wiring lines O, O' of Yamashita correspond to the common terminal pads of claim 25" and "Yamashita does not teach or suggest such common output terminal pads" and "Fig. 3b of Yamashi relied upon by the examiner shows no such terminal pads". However, C200, Fig. 3b of Yamashita et al. does show the source electrode or the drain electrode of each of the transistors (T200, T201, T202, T203) being electrically in contact with the common output terminal pads (O,O') wherein the output signals O,O' are the common output terminal pads of its circuitry 200. Since claims 1,25

do not recite a first common output terminal pad being directly electrically in contact with the source electrode or the drain electrode of the first transistor and directly electrically in contact with the source electrode or the drain electrode of the second transistor, the two electrodes of the first and second transistors which are directly electrically in contact with the first common output terminal pad not being connected to any of the input terminal pads; a second common output terminal pad being directly electrically in contact with the source electrode or the drain electrode of the third transistor and being directly electrically in contact with the source electrode or the drain electrode of the fourth transistor, the two electrodes of the third and fourth transistors which are directly electrically in contact with the second common output terminal pad not being connected to any of the input terminal pads, applicant's claims 1,25 do not distinguish over Yamashita et al. reference.

It is argued, at page 10-12 of the remark, that "Yamashita and prior art description in the specification individually to show that none of the references provides the motivation to combine them"; "applicants request examiner to provide specific evidence in the prior art of a motivation to combine Yamashita and the prior art description in the specification despite the difficuilty explained above" and "applicants request the examiner to provide evidence that persons of ordinary skill in the art would have included two SPDT switches into Yamashita's logic circuit in the manner recited in claim 27". However, in response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art.

See In re Fine, 837 F.d. 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and In re Jones, 958 F.d. 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the applicant made the erroneous assumption that the motivation to combine must be expressly stated in the art of record. From MPEP § 2144:

> "The rationale to modify or combine the prior art does not have to be expressly stated in the prior art; the rationale may be expressly or impliedly contained in the prior art or it may be reasoned from knowledge generally available to one of ordinary skill in the art, established scientific principles, or legal precedent established by prior case law. In re Fine, 837 F.d. 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.d. 347, 21 USPQ2d 1941 (Fed. Cir. 1992). See also In re Eli Lilly & Co., 902 F.d. 943, 14 USPQ2d 1741 (Fed. Cir. 1990) (discussion of reliance on legal precedent); In re Nilssen, 851 F.d. 1401, 1403, 7 USPQ2d 1500, 1502 (Fed. Cir. 1988) (references do not have to explicitly suggest combining teachings); Ex parte Clapp, 227 USPQ 972 (Bd. Pat. App. & Inter. 1985) (examiner must present convincing line of reasoning supporting rejection); and Ex parte Levengood, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993) (reliance on logic and sound scientific reasoning)." [Emphasis added]

In the present case, the examiner has presented a line of reasoning supporting his motive to combine which was expressly stated in the rejection in the last office action and is expressly stated in the rejection below. The applicant cannot rebut the examiner's arguments simply by making the inaccurate statement that the examiner has provided no line of reasoning for the applicant to rebut.

Conclusion

5. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Tan Tran whose telephone number is (703) 305-3362. The examiner can normally be reached on M-F 8:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for after final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

TT

Nov 2003

Minhloan Tran
Primary Examiner
Art Unit 2826